Monolithic Integration of GaN Transistors for Higher Efficiency and Power Density in DC-DC Converters

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Abstract

Power converters are constantly trending towards higher output power, higher efficiency, and higher power density. To provide improved performance better power devices are required. For silicon (Si) power devices, the gains in performance have slowed as the technology has matured and approaches its theoretical limits [1]. Gallium nitride (GaN) devices have emerged as a possible replacement for silicon devices in various power conversion applications and as an enabler of new applications not previously possible [1]-[4]. In this paper we will discuss the latest eGaN® FETs developments, including a major improvement with the latest generation of discrete devices and introduce a new family of monolithic half bridge ICs offering unmatched high frequency performance. These new families of eGaN FETs are widening the performance gap with the aging power MOSFET in high frequency power conversion by providing significant gains in key switching figures of merit, continued reductions of performance limiting in-circuit parasitics, and improved thermal performance.

1. Rapid Improvements in GaN Performance

The GaN technology journey is just beginning, and we are still far from theoretical performance limits [1]. It is quite reasonable to expect a rapid rate of improvement reminiscent of Moore's Law, which predicted the growth of microprocessor technology – doubling of product performance every two to four years for at least the next decade. The latest generation (circa 2014) of discrete high current eGaN FET power transistors demonstrates over a two-fold reduction in hard switching figure of merit (FOM_{HS}) [5] over the previous generation (circa 2011), as shown on the left in figure 1. The latest generation of eGaN FETs also have over a two-fold reduction in on-resistance compared to their predecessor, increasing the current capability of GaN transistors [5]. The latest generation family of eGaN FETs, when compared to the state-of-art Si power MOSFETs, reduces FOM_{HS} by 4.8 times, 8 times, and 5 times respectively for 40 V, 100V, and 200 V devices as plotted on a log scale shown on the right in figure 1.

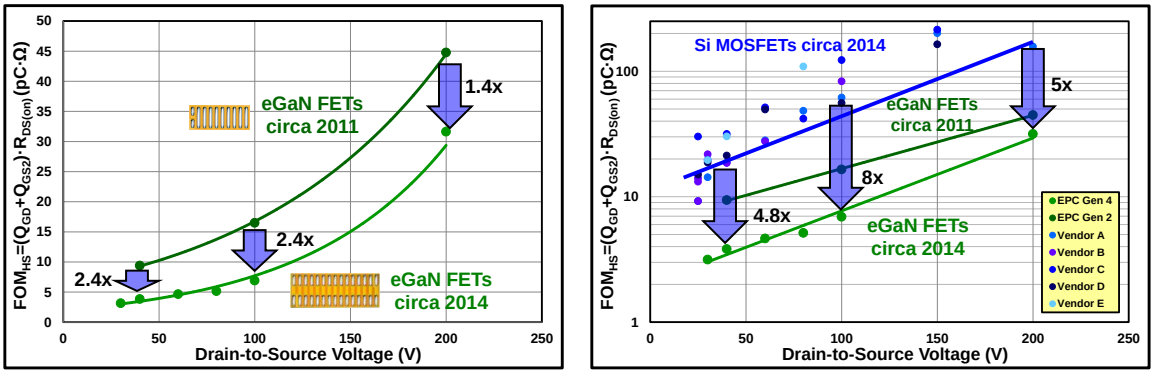
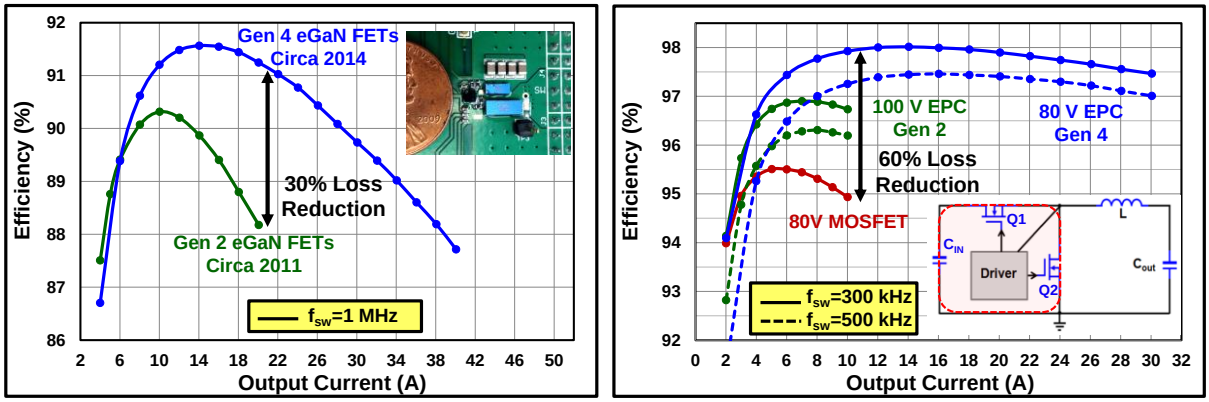


Fig.1. Hard switching FOM_{HS} comparison of generation 2 (circa 2011) and generation 4 (circa 2014) high current eGaN FETs (left) and eGaN FETs and state-of-the-art Si MOSFETs (right) for drain-to-source voltages at half of the rated voltage, and a drain-to-source current of 20 A

The rapid improvement in device performance directly correlates to better in-circuit performance. To highlight the improved performance of the latest generation 4 high current eGaN FETs in lower voltage point of load (POL) applications, a buck converter was built using a combination of generation 4 eGaN FETs as the synchronous rectifier (SR) and generation 2 eGaN FETs as the control device (inset on the left of figure 2). The converter combined the 30 V EPC2023 (generation 4) with the 40 V EPC2015 (generation 2) in a V_{IN} =12 V to V_{OUT} =1.2 V DC-DC POL converter. Shown on the left of figure 2 are the experimental system efficiencies of the 12 V to 1.2 V, 40 A POL converter operating with a switching frequency of 1 MHz achieving efficiencies above 91.5% and demonstrating the superior in-circuit performance of generation 4 eGaN FET power devices (shown in blue) compared to generation 2 eGaN FETs (shown in green). At 1 MHz and 20 A, the generation 4 based eGaN FET design can reduce the system power loss, which includes the inductor and driver losses, by over 30% when compared to the generation 2 GaN based design, and the output current can be increased to 40 A, where an efficiency just below 88% is achieved.



V_{IN} =12 V V_{OUT} =1.2 V V_{IN} =48 V V_{OUT} =12 V

Fig.2. Experimental system efficiency comparison between eGaN FET based buck POL converters (left), V_{IN} =12 V to V_{OUT} =1.2 V, f_{SW} = 1 MHz, (blue: generation 4 eGaN FET curve, Top Switch (Q1): EPC2015, Synchronous rectifier (Q2): EPC2023, Inductor (L): Wurth 744309025; green: generation 2 eGaN FET curve, Q1: EPC2015, Q2: EPC2015, L: Wurth 744306030) and EPC9018 generation 4 half bridge development board (inset). Experimental system efficiency comparison between GaN and Si based non-isolated buck intermediate bus converters (right), V_{IN} =48 V to V_{OUT} = 12 V, f_{SW} =300 kHz and f_{SW} =500 kHz (blue: generation 4 eGaN FET curve, Q1: EPC2021, Q2: EPC2021, L: Coilcraft SER2915L-472KL; green: generation 2 eGaN FET curve, Q1: EPC2001, Q2: EPC2001, L: Coilcraft SER1390-103ML; red: Si MOSFET curve, Q1: BSZ123N08NS3 G, Q2: BSZ123N08NS3 G, L: Coilcraft SER1390-103ML) and (inset) buck converter schematic with high frequency power loop highlighted in red

As the voltage across the transistor increases so to do the switching related losses. For higher voltages, the device FOM also worsens, shown in figure 1, as the device structure changes to block a higher voltage. As the voltage requirement for a high frequency application increases, so does the advantage of the GaN transistors due to their ability to significantly reduce switching losses when compared to Si MOSFETs. Shown on the right of figure 2 are the experimental system efficiencies of the 48 V to 12 V, 30 A non-isolated buck intermediate bus converters operating at a switching frequency of 300 kHz. The generation 4 eGaN FET based design achieves efficiencies above 98% demonstrating the superior in-circuit performance of generation 4 eGaN FET power devices (shown in blue) compared to generation 2 eGaN FETs (shown in green), and Si MOSFETs (shown in red). At 300 kHz and 10 A, the eGaN FET design can reduce the system power loss, which includes the inductor and driver, by 60% when compared to the MOSFET design. With the improved performance provided by eGaN FETs, higher frequency can be achieved without significantly sacrificing efficiency. Also shown on the right of figure 2 are the efficiencies of the 48 V to 12 V GaN based buck converters operating at switching frequencies of 500 kHz.

2. Reducing Parasitics to Maximize GaN Performance

As GaN power devices rapidly improve, the parasitics introduced by the package and printed circuit board (PCB) must continually be reduced to enable the high speed switching of the GaN power device and maximize in-circuit performance [6]-[10]. GaN transistors' chipscale LGA package have significantly lower package inductance than Si MOSFETs. Lower package inductance minimizes the parasitic di/dt voltage bumps, voltage overshoot, and maximizes switching speed as shown on the left in figure 3. To minimize the PCB inductance an optimized layout for GaN transistors was developed and total high frequency loop inductances under 400 pH were achieved [10]. The high frequency power loop, shown on the right in figure 2, is comprised of the parasitic inductance of the input capacitors, top device (Q1), synchronous rectifier (Q2), and PCB traces connecting these components. The eGaN FET based half bridge high frequency loop inductance is much lower than the conventional Si MOSFET design, which was measured from the waveform in figure 3 to be approximately 2.5 nH. For the latest generation of eGaN FET PCB designs [11], with an example shown on the right in figure 3, the vias, which were previously located outside of the device, now have been filled and placed underneath the device, reducing the space between the dies and further reducing parasitic total high frequency parasitic loop inductance to approximately 250 pH. The high frequency parasitic loop inductances were experimentally measured by using the resonant frequency of the ringing voltage after the top switch turns on. When the top switch turns on, the parasitic high frequency loop inductance and output capacitance of the synchronous rectifier ring at the resonant frequency, yielding:

$$L_{Loop} = \frac{T_{Ring}^{2}}{4 \cdot \pi^{2} \cdot C_{OSS}} \quad (1)$$

Where L_{LOOP} is the high frequency loop inductance, T_{RING} is the ringing period, and C_{OSS} is the output capacitance of the synchronous rectifier.

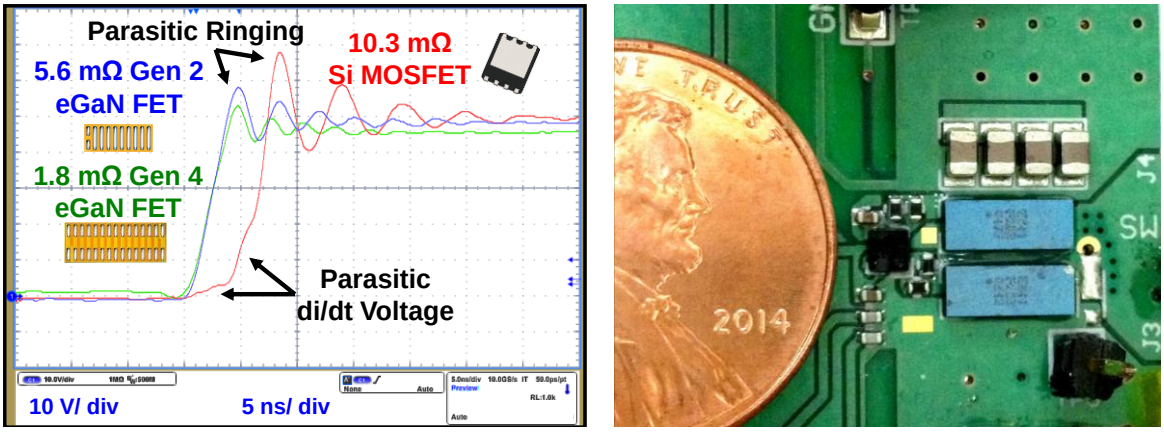
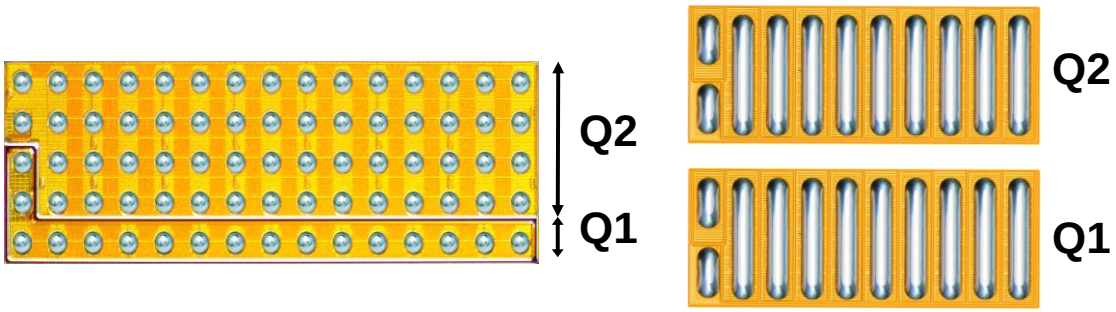


Fig. 3. Switching node waveforms of eGaN FET and MOSFET designs (left) (V_{IN}=48 V, I_{OUT}=10 A, f_{sw}=300 kHz, generation 4 GaN transistors: EPC2021, generation 2 GaN transistors: EPC2001, MOSFETs: BSZ123N08NS3G) and EPC9034 generation 4 half bridge development board [11] (right)

3. Integrating GaN for Improved High Frequency Performance

Beyond device level and design improvements, the greatest opportunity for lateral GaN technology to impact power conversion comes from its intrinsic ability to integrate multiple devices on the same substrate. In the future, GaN will allow designers to implement higher voltage monolithic power systems on a single chip in a more straightforward and cost-effective manner, as opposed to current silicon multi-chip solutions [6], which have higher complexity, lower performance, and higher cost.

Today, the most common building block used in power conversion is the half bridge. This therefore becomes the starting point for the journey towards a power system-on-a-chip. On the left in figure 4 is a picture of the first commercially available enhancement mode monolithic half bridge (HB) GaN IC. In each of the first three members of the family of half bridge ICs, with rated voltages of 30 V, 60 V, and 80 V available, the high side FET is approximately one-fourth the size of the low side device to optimize efficient DC-DC conversion with a high V_{IN}/V_{OUT} step down ratio common in buck converters (also available for higher duty cycles are half bridges with a one to one sizing ratio of the top (Q1) and bottom (Q2) device). The table of available monolithic half bridge GaN ICs and device parameters are shown on the bottom of figure 4.



Part Number	Configuration	V_{DS}		Max $R_{DS(ON)}$ (mΩ) @5V_{GS}	Q_G typ (nC)	Q_{GS} typ (nC)	Q_{GD} typ (nC)	Q_{OSS} typ (nC)
EPC2100	Dual Asymmetric	30	Q1 Q2	8 2	3.5 15	1.4 4.6	0.57 2.6	5.5 28
EPC2101	Dual Asymmetric	60	Q1 Q2	11.5 2.7	2.7 12	1 3.7	0.50 2.5	9 45
EPC2102	Dual Symmetric	60	Q1 Q2	4.4	6.8	2.3	1.4	23 31
EPC2103	Dual Symmetric	80	Q1 Q2	5.5	6.5	2.0	1.3	29 39
EPC2105	Dual Asymmetric	80	Q1 Q2	14.5 3.4	2.5 10	1 3.2	0.50 2	11 55

Fig. 4. Two eGaN FETs integrated onto one chip forming a monolithic half bridge (top left) compared to two discrete eGaN FETs (top right), both in chipscale packages (Bump Side) and table of monolithic half bridge GaN ICs and device parameters

In figure 5, a top view pin-out configuration of the asymmetric half bridge is shown. Gate 1 is the high side gate pin. GR1 is the high side gate return pin. Gate 2 is the low side gate pin. V_{SW} is the switch node of the half bridge and consists of 35 solder bumps. V_{IN} is the input voltage supplied to the drain of the top FET (Q1), and consists of 8 solder bumps. P_{GND} is the power ground connection at the source terminal of the lower FET (Q2) and has 29 solder bumps. By integrating the two power FETs into a single monolithic device, the space needed on the PCB, as shown on the right in figure 5, is significantly reduced.

The monolithic half bridge GaN IC is the same size as a single discrete generation 4 eGaN FET and provides a smaller total solution size than a half bridge with two discrete generation 2 eGaN FETs, as shown on the upper right in figure 4. The monolithic half bridge GaN IC has the latest eGaN FET device FOM improvements and the lowest parasitic inductances and is a suitable replacement for discrete generation 2 eGaN FET based half bridge designs. In figure 6, the experimentally measured high frequency loop inductances

of various generations of eGaN FET based half bridge designs are compared, with the monolithic half bridge GaN IC based design having an ultra-low inductance value of around 150 pH. The asymmetric monolithic half bridge GaN IC, when compared to high current discrete generation 4 eGaN FETs, is designed for higher frequency, lower current, and higher step down applications.

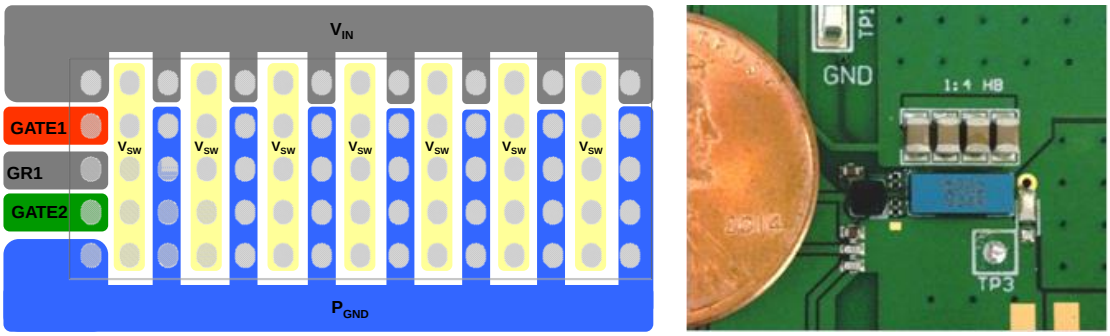


Fig. 5. Top view pin-out configuration for the asymmetric monolithic half bridge device (left) and EPC9036 asymmetric monolithic half bridge demonstration board [12] (right)

GaN Based Half Bridge Design	High Frequency Loop Inductance
Discrete Generation 2 eGaN FETs [10]	**0.4 nH**
Discrete Generation 4 eGaN FETs [11]	**0.25 nH**
Integrated Monolithic Half Bridge GaN IC [12]	**0.15 nH**

Fig. 6. Table of approximate high frequency loop inductances for generations of eGaN FET based half bridge designs

The measured efficiency of the 30 V monolithic half bridge eGaN IC in a low voltage point of load (POL) buck converter is shown in figure 7. At 1 MHz, peak system efficiencies, which includes the inductor and driver losses, of the monolithic eGaN FET HB-based buck converter approaches 91% at 10 A, and, at 20 A, the efficiency is over 89.5%. At a switching frequency of 4 MHz, the efficiency exceeds 81% at 20 A. The integrated monolithic eGaN FET HB design has the benefit of being able to properly size the devices without increased package parasitics, allowing for a smaller control FET (Q1) to reduce the switching related losses, and a larger synchronous rectifier (Q2) to reduce conduction losses, each the respective dominant loss mechanism for devices Q1 and Q2. Faster switching speeds, enabled by the low FOM and system parasitics, along with die size optimization, are shown on the right in figure 7. The switching node of this 30 V half bridge eGaN IC exhibits rising and falling times of faster than 1 ns and approximately 1 ns, respectively.

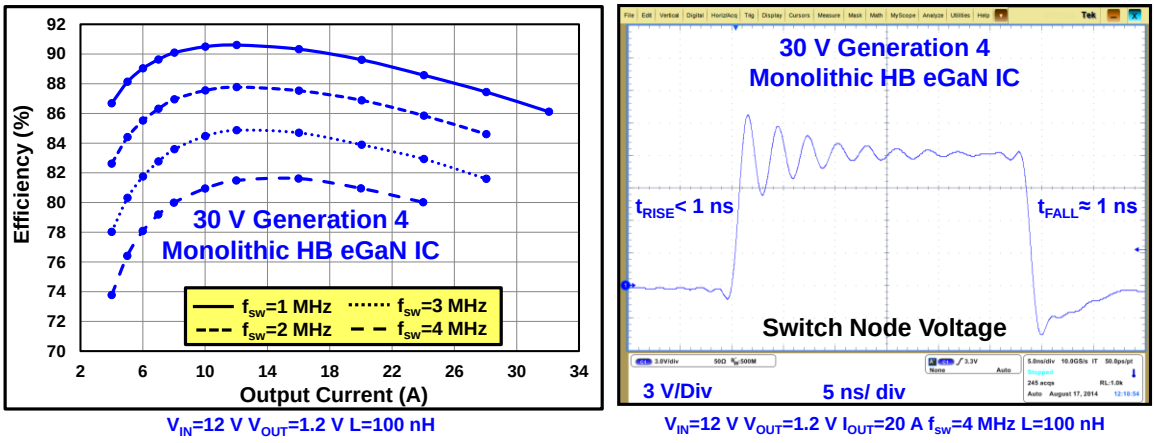


Fig. 7. Total 12 V_{IN} to 1.2 V_{OUT} buck converter efficiency of 30 V EPC2100 monolithic half bridge GaN IC (left) (V_{IN}=12 V, V_{OUT}=1.2 V, L: Coilcraft SLC7649S-101KL, gate driver: LM5113) and switching node waveform at f_{SW}=4 MHz and I_{OUT}=20 A (right)

Going to even higher input voltage and higher step down ratios for POL conversion, the advantages of integration become greater. On the left of figure 8 is the efficiency of a buck converter running at 300 and 500 kHz with the EPC2105. This 80 V half bridge eGaN IC can convert 48 V directly to 1 V efficiently. At 16 A, peak efficiency of over 80% is achieved for the full buck converter system at 500 kHz. At 300 kHz, the full converter efficiency is 84 % at 16 A. This conversion eliminates two stages that are normally required for this voltage conversion in Datacom systems. The switching node of this 80 V half bridge eGaN IC, shown on the right in figure 8, exhibits rising and falling times of approximately 2 ns.

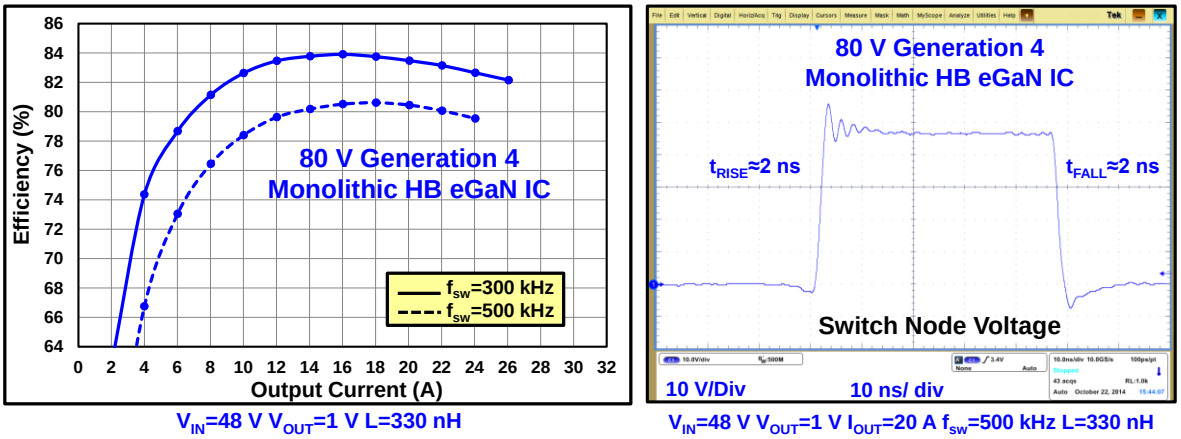


Fig. 8. Total 48 V_{IN} to 1 V_{OUT} buck converter efficiency of 80 V EPC2105 monolithic half bridge GaN IC (left) (V_{IN}=48 V, V_{OUT}=1 V, L= Wurth 744301033) and switching node waveform at f_{sw}=500 kHz and I_{OUT}=20 A (right)

4. Improving Thermal Performance

Combined with the increasing current density and switching speeds, power devices must be accommodated in an ever decreasing board space and therefore must also become more thermally efficient. A high density power device must not only be more electrically efficient by generating less heat, but also enable superior thermal conduction properties.

The thermal efficiency of a package can be determined by comparing the two parameters, $R_{\Theta JC}$ and $R_{\Theta JB}$, normalized to the package area. $R_{\Theta JC}$ is the thermal resistance from junction-to-case, this is the thermal resistance from the active part of the eGaN FET to the top of the silicon substrate, including the sidewalls. $R_{\Theta JB}$ is the thermal resistance from junction-to-board, this is the thermal resistance from the active part of the eGaN FET to the printed circuit board. For this path the heat must transfer through the solder bars to the copper traces on the board. In figure 9 is a compilation of thermally related characteristics for several popular surface mount MOSFET packages as well as two popular eGaN FETs.

Device Package	$R_{\Theta JC}$ ($^oC/W$)	$R_{\Theta JB}$ ($^oC/W$)	Area (mm^2)
Blade [13]	1	1.6	10.2
CanPAK S [14]	2.9	1	18.2
CanPAK M [15]	1.4	1	30.9
S308 [16]	-	1.8	10.9
S308 Dual Cool [17]	3.5	2.7	10.9
Super SO8 [18]	20	0.9	30.0
Super SO8 Dual Cool [19]	1.2	1.1	30.0
EPC2001c eGaN FET [20]	**1.0**	**2.0**	**6.7**
EPC2021 eGaN FET [21]	**0.5**	**1.4**	**13.9**
EPC2105 eGaN FET [22]	**0.4**	**1.3**	**13.9**

Fig. 9. Comparison of package area and thermal resistance components $R_{\Theta JC}$ and $R_{\Theta JB}$

On the left in figure 10 shows a plot of the junction-to-board resistance ($R_{\Theta JB}$) for each of the packages given in figure 9. Red square dots represent the MOSFET packages, and blue circular dots represent the eGaN FETs. The majority of the sampled packages fall on a single trend line indicating that performance for this element of thermal resistance is determined primarily by package size, and not technology. In contrast, on the right in figure 10 shows a plot of the thermal resistance from junction to case ($R_{\Theta JC}$). The CanPAK and double-sided cooling SO8 packages are far less efficient at extracting the heat out of the top of the package than either the Blade package or the eGaN FETs. The eGaN FETs, however, are over 30% lower than even the Blade [13] when normalized to the same area. This makes the eGaN FETs the most efficient thermal package for double sided cooling and most suitable for high density power designs.

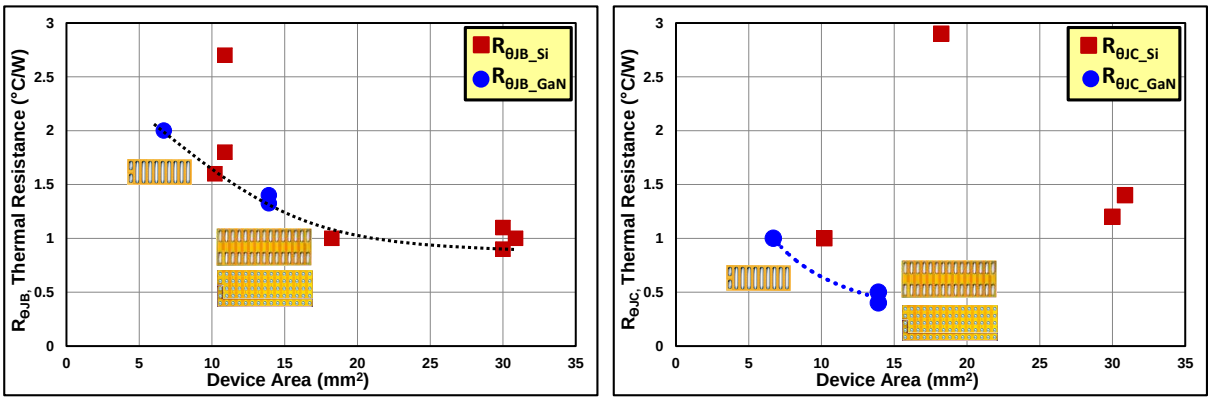


Fig. 10. $R_{\Theta JB}$ (Junction-to-Board Thermal Resistance) (left) and $R_{\Theta JC}$ (Junction-to-Case Thermal Resistance) (right) for several package styles listed in figure 9, eGaN FETs represented by blue circular dots and Si MOSFETs represented by red square dots

5. Conclusions

GaN transistors have been available in production for almost 5 years and have already demonstrated their superior high frequency performance compared to Si MOSFETs. As GaN transistors continue to rapidly improve on the device level, the packaging and surrounding parasitics must also be continually improved to achieve the best in-circuit electrical and thermal performance. This paper introduced the first family of commercially available enhancement mode monolithic half bridge GaN ICs and explored the fundamental reasons for the improved performance provided by monolithically integrating GaN transistors. These monolithic half bridge GaN ICs are the starting building blocks to more efficient high frequency power conversion and just the beginning of the journey towards a GaN based high voltage power system-on-a-chip.

6. References

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